



Exhibit 31



Scott Matlock · 3rd

Lead Debugger for System level issues on 5G Baseband and Radio products

-  Ericsson
-  University of Houston-Clear Lake

Austin, Texas, United States · [Contact info](#)

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Experience



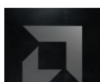
Debug Lead

Ericsson · Full-time

Sep 2022 - Present · 7 mos

Austin, Texas Metropolitan Area · On-site

Debug Lead for 5G Baseband and Radio ASICs



AMD

5 yrs 4 mos



Director Design Engineering

Full-time

Sep 2021 - Sep 2022 · 1 yr 1 mo

Austin, Texas Metropolitan Area · On-site

Managed a team of 15-20 validation and debug engineers working on Client PC products

Role included:

Debugged critical System Level issues blocking production of Mobile platforms

Managed a team of debuggers working on next generation mobile platforms. This included managing dozens of issues in parallel

Managed a team of validation engineers creating and executing system validation plans for Mobile products

Director, Design Engineering

Full-time

Jul 2019 - Sep 2021 · 2 yrs 3 mos

Austin, Texas Metropolitan Area · On-site

Director, Design Engineering at AMD

Lead System Engineer leading a team of 50+ engineers to test and validate a unique low power APU

Duties include:

- Work with the engineering teams to create test plans to fully cover customer H/W and S/W use cases
- Drive alignment between H/W validation, Firmware development, Android OS development, and Software QA and test
- Review and align all Silicon coverage test plans
- Work with Business and Production teams to align validation and production streams
- Work with customer to address critical validation and H/W compliance issues
- Work with System Program Management to complete all AMD validation work threads
- Drive all critical program observations to root cause and help in developing workarounds and fixes

Director Design Engineering

Jun 2017 - Jul 2019 · 2 yrs 2 mos

Austin, Texas Area

Technical Lead for Tier 1 Graphics customer. Duties include:

- Lead a team of Application Engineers in three geographic regions
- Provide Design, Debug, and Platform Engineering support to the customer
- Drive all gating H/W issues to resolution before product production

Senior Staff Engineer

Samsung Austin R&D Center (SARC)

Mar 2015 - Jun 2017 · 2 yrs 4 mos

FM2222 in Austin Tx

****SARC IP Design Debug****

...

[...see more](#)**AMD**

9 yrs 5 mos

Principle Member Technical Staff

Sep 2011 - Mar 2015 · 3 yrs 7 mos

Advanced Micro Devices, Austin

Served as a technical lead to validate and enable APU products for the Ultra Low Power (ULP) market segment. This includes:

- Helped to define feature sets of the APU with a focus on platform cost and power reduction
- Helped to architect a reference platform to showcase the unique features of the ULP APU
- Helped to architect a validation platform to effectively test, debug, and characterize a ULP APU
- Led a team of validation architects to ensure all critical APU features were fully validated
- Worked with Customer Enablement teams to ensure platform feature sets were properly documented so customer design teams could optimize their platforms for performance and power.
- Represented the Platform Engineering organization in technical syncs with OS vendors, third party H/W and S/W vendors

Senior Member Technical Staff

Nov 2005 - Aug 2011 · 5 yrs 10 mos

Austin, Texas Area

Technical lead (manager) of eight engineers in the system debug department.

- Responsible for all external customer issues (Server, Desktop, and Notebook)
- Provided detailed resolution reports back to the customer
- Provided H/W fixes, BIOS, S/W and OS patches as necessary to the customer
- Mentored the younger engineers on technical subjects as well as providing advice on career advancement

**Hewlett-Packard**



8 yrs 6 mos

Houston, Texas Area

Engineer V

May 2003 - Oct 2005 · 2 yrs 6 mos

****Server Storage Design Group****

...

[...see more](#)

Engineer IV

May 1997 - Apr 2003 · 6 yrs

****Industry Standard Servers (ISS) Hardware Engineering Problem Resolution (EPR) group**...**

[...see more](#)

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Education



University of Houston-Clear Lake

Bachelor of Science (BS), Computer Engineering

2001 - 2005

Grade: Graduated Summa Cum Laude 3.98 GPA

Activities and societies: Member of Alpha Chi (National College Honor Society)



San Jacinto College

General Studies, Pre Engineering

1997 - 2001

Grade: GPA 3.95

Activities and societies: Member of Phi Theta Kappa (National Junior College Honor Society)

Skills

RTL design



2 endorsements


Semiconductors




Endorsed by 8 colleagues at AMD



2 endorsements

 8 endorsements

DFT

 1 endorsement[Show all 50 skills →](#)

Recommendations

Received

Given

**Somas Thyagaraja**  · 3rd

Director, Product Management at SoFi

April 29, 2014, Somas reported directly to Scott

Scott is without doubt one of the best managers I have ever had. He has never hesitated to share his technical expertise and assist me on issues I was debugging while at AMD. His professional attitude, hardworking nature, and analytical approach to solving problems are all qualities I've observed and...

Patents

Emulated legacy bus operation over a bit-serial bus

US 9,858,235 · Issued Jan 2, 2018

EMULATED KEYBOARD CONTROLLER AND EMBEDDED CONTROLLER INTERFACE VIA AN INTERCONNECT INTERFACE

US 20140006645 · Filed Jul 12, 2012

[See patent](#)

Low cost alternative to connect a PC compatible EC to an I2C bus. This eliminates the need to have an antiquated LPC bus on the I/O bridge.

Interests

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**AMD**

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San Jacinto College

74,937 followers

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PMTS - Lead System Engineer at AMD


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Senior Systems Design Engineer at AMD


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Allan Parker • 2nd

AMD Fellow x86 Client Platform Engineering

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Krish Venkatachalam • 3rd

Director Design Engineering at AMD

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6 of 7

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Marketing and Communications Coordinator at Robins Kaplan LLP

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Marc Betinsky

Partner at Robins Kaplan LLP

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